40GBASE–SR4 QSFP+ Optical EnginePreliminary

Features:

- High-speed and high-performance Data Communication applications
- Fiber Channel Networking/Storage applications

Applications:

- 40GBASE–SR4 QSFP+ Transceiver and Active Optical Cable

Specifications:

Absolute Maximum Ratings

Parameter	Symbol	Min	Max.	Unit
LD Reverse Voltage	$Vr_{(LD)}$	--	5	V
LD Forward Current	$If_{(LD)}$	--	12	mA
Operating Temperature	Top	-0	70	℃
Storage Temperature	Tstg	-40	85	℃
Lead Solder Temperature	--	--	260	℃
Lead Soldering Time	--	--	2	s

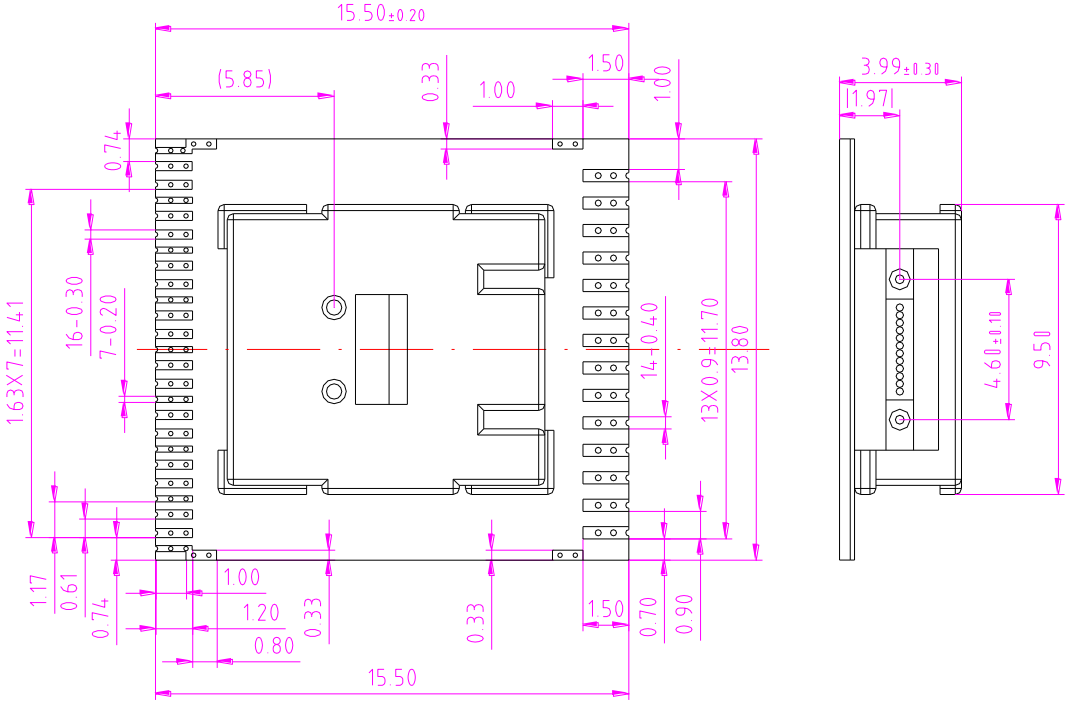
Transmitter Optical& Electrical Characteristics (T=25ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Threshold Current	Ith	25℃	--	1.0	1.5	mA
Forward Voltage	Vf	Iop=6.5mA	--	1.9	--	V
Central Wavelength	λc	Iop=6.5mA	840	850	860	nm
Spectral Width(RMS)	Δλ	Iop=6.5mA	--	--	0.60	nm
Average launch power, each lane	Po	Iop=6.5mA	-7.6	--	2.4	dBm
Optical Modulation Amplitude (OMA), each lane	--	--	-5.6	--	3	dBm
Difference in launch power between any two lanes (OMA)	--	Iop=6.5mA	--	--	4	dB
Extinction ratio	ER	Iop=6.5mA	3	--	--	dB
Optical Return Loss	ORL	--	--	--	-12	dB
Average launch power of OFF transmitter, each lane	--	--	--	--	-30	dBm

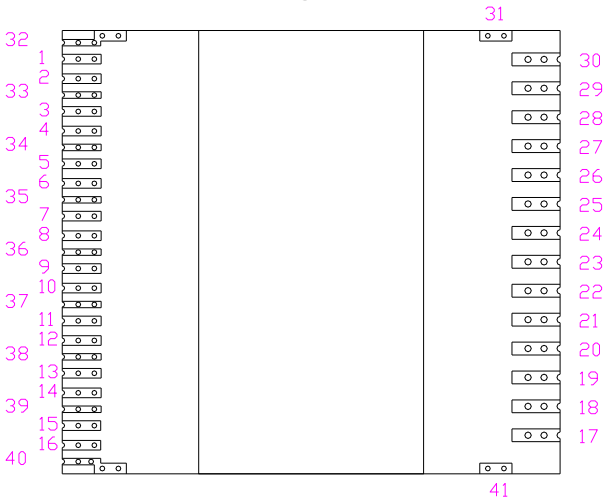
Receiver Optical/Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Damage threshold	--		3.4	--	--	dBm
Average power at receiver input, each lane		10.3125Gbps, PRBS31, BER=1*E-12 , ER=4.5dB, Output Differential Voltage = Min.290mV	-9.5	--	2.4	dBm
Optical Return Loss	ORL	--	--	--	-12	dB
Optical Modulation Amplitude (OMA), each lane	--	--	--	--	3	dBm
Peak Power, each lane	--	--	--	--	4	dBm

Outline Dimension(mm) :

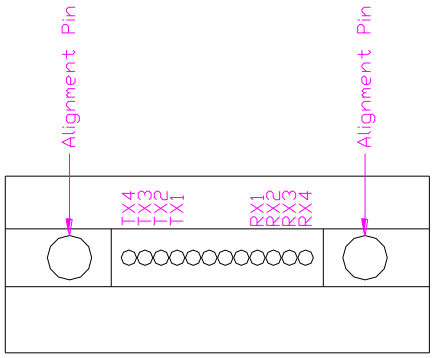


Electrical IO Assignment:



Top View

Optical IO Assignment:



Front View

Pin Number	Pin Name	Description
1	DOUT4N	Differential high-speed Data Output pads, P is the positive (non- inverted) node and N is the negative (inverted) node.
2	DOUT4P	
3	DOUT3N	
4	DOUT3P	
5	DOUT2N	
6	DOUT2P	
7	DOUT1N	
8	DOUT1P	
9	DIN1P	Differential high- speed Data Input pin P is the positive (non-inverted) node and N is the negative (inverted) node. The differential inputs are internally terminated with 100Ω. Pin P is the positive (non- inverted) node and pin N is the negative (inverted) node.
10	DIN1N	
11	DIN2P	
12	DIN2N	
13	DIN3P	
14	DIN3N	
15	DIN4P	
16	DIN4N	

17	NOTINTT	The active- low Interrupt (NOTINT) signal notifies the external microcontroller about driver events. These events include VCSEL operating voltage violations (VVL_x, VVH_x), input loss of signal, input signal detect and control loop faults. The polarity of the interrupt can be inverted by programming. The state of the pin may be read through the management interface.
18	SDAT	The Serial Data pin (SDA) is a bidirectional pin for the data signal. The pin can be tied directly to VDD of 3.3V or 2.5V. The SDA pin is I^2C- bus compatible. This pad is a CMOS input/output pad. The pullup is 10 kΩ.
19	SCLT	The Serial Clock pin (SCL) is the clock signal of the serial interface. The pin can be tied to VDD 3.3V or 2.5V. The SCL input is I^2C- bus compatible and can be clocked at up to 1000kHz. The pullup is 10kΩ.
20	IMON	The Monitor Current output (IMON) is an analog output with two functions. The IMON Select Register controls a multiplexer to select either a scaled replica of the unit current, a temperature proportional current, or, a scaled copy of the average current of a specific channel. By measuring the unit current during production, process dependencies are isolated and an estimate of the settings can be calculated. The average current and modulation current are derived from the unit current (I_U). The copy of the average current of an individual channel is used for real time diagnostic functions. The output is connected to ground via a resistor. A microcontroller with an integrated analog to digital converter can monitor this output and service queries from the host system.

21	LDIS	The Laser Disable pin (LDIS) is a global output disable signal that will set Iavg and Imod to 0 when it is high, regardless of other settings. The pin can be left unconnected and the device will operate normally.The state of the pin may be read through the management interface.
22	VCCT	Positive supply of driver stages and VCSEL anodes
23	GNDT	Negative supply, substrate
24	GNDR	Negative supply, substrate
25		
26	VCCR	Positive supply of TIA stage and Limiting amplifier stage
27	RSSI	The Receiver Signal Strength Indicator output (RSSI) pad is an analog output that sources a current proportional to the average photo- detector current on the selected channels. The output is used during manufacturing for active alignment. As well, the output can be configured to produce a temperature proportional output.
28	NOTINTR	The active- low Interrupt (NOTINT) signals notifies the microcontroller about signal detect events such as signal detect and loss of signal when the events are unmasked. In systems using polling-based firmware, this input may be left unconnected.
29	SCLR	The Serial Clock pad (SCL) is the clock input signal of the serial interface. The pad can be tied to VDD of 3.3V or 2.5V via a resistor. The SCL input is I^2C-bus compatible and operates at up to 1000kHz. If the serial interface is unused, this pad should be left unconnected.
30	SDAR	The Serial Data pad (SDA) is a bidirectional pad for the serial data signal. The pad can be tied to VDD of 3.3V or 2.5V via a resistor. The SDA pad is I^2C-bus compatible and operates at up to 1000kHz. If the serial interface is unused, this pad should be left unconnected.

31	GNDR	Negative supply, substrate
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36	GNDT	Negative supply, substrate
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Order Information:

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Statement:

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